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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,365	12/01/2003	Mitsuaki Osame	12732-183001 / US6776	8069
26171	7590	03/10/2006	EXAMINER	
FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			NGUYEN, LONG T	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/724,365

Applicant(s)

OSAME ET AL.

Examiner

Long Nguyen

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) See Continuation Sheet is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 65-96 is/are allowed.
- 6) ☒ Claim(s) 1,2,14,15,24,25,37,38,47,48 and 57-64 is/are rejected.
- 7) ☒ Claim(s) 7,8,11,12,20,21,30,31,43,44,53 and 54 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 June 2005 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/20/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1,2,7,8,11,12,14,15,20,21,24,25,30,31,37,38,43,44,47,48,53,54 and 57-96.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/20/05 has been entered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 2, 14, 15, 24, 25, 37, 38, 47, 48 and 57-64 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 8 of U.S. Patent No. 6,870,895. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 8 of U.S. Patent No. 6,870,895 recites a circuit that

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includes a digital signal (clock signal) a capacitor (line 3 of claim 7), an inverter (line 4 of claim 7), a switch (line 7-8 of claim 7), the switch is ON and a first potential is input to the second electrode of the capacitor (line 17-23 of claim 7), wherein the digital signal is input to the second electrode of the capacitor during the sampling period (line 24-26 of claim 7), and wherein the first potential is one of a high level and a low level of the digital signal (line 3-4 of claim 8) which meets the limitations of pending independent claims 1 and 57. Note that, claim 8 of U.S. Patent No. 6,870,895 also recites first means and second means for connecting (lines 9-12 of claim 7), and it is obvious to one skill in the art to use a switch as a means for connecting because a switch is easily controlled to be connected/disconnected, and thus it also meets the limitations first switch (a switch on line 7-8 of claim 7), a second switch (switch that is used for second means for connecting) and a third switch (switch that is used for third means for connecting) recited in pending independent claims 2 and 61. Note that, for dependent claims 14, 24, 37, 47, 58-60 and 62-64, they are also meet by the Patent 6,870,895 because the reset period (lines 17-23 of claim 7) and the sampling period (clock receiving period, line 24-26 of claim 7) are determined by respective first and second sampling pulses from respective first and second delayed flip-flops are intended use and are not part of the data latch circuit (for claim 14 and 15); for claims 24, 2558 and 62, it is also obvious that the amplitude between the high and low level of the digital signal is smaller than an amplitude of an output of the inverter because the circuit of claim 8 of U.S. Patent No. 6,870,895 is a level shifter circuit, and it is known in the art that a level shifter circuit can be used to shift a signal form a lower voltage to a higher voltage or vice versa depending on the need of the designer; for claims 37, 38, 59 and 63, it is obvious to use thin film transistors for the circuit for the purpose of saving space; and for claims 47, 48, 60 and

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64, the limitation that the circuit/device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone a navigation system and a camera is an intended use and the circuit of U.S. Patent No. 6,870,895 capable of selecting from that group.

Claim Objections

4. Claims 1, 2, 7, 8, 11, 12, 14, 15, 20, 21, 24, 25, 30, 31, 37, 38, 43, 44, 47, 48, 53 and 54 are objected to because of the following informalities:

Claim 1, line 7, “means” should be deleted (see line 2 of claim 1).

Claims 14, 24, 37 and 47 are objected to because they include the informality of claim 1.

Claim 2, line 10, “means” should be deleted (see line 2 of claim 2).

Claims 15, 25, 38 and 48 are objected to because they include the informality of claim 2.

Claim 7, line 10, “means” should be deleted (see line 2 of claim 7).

Claims 11, 20, 30, 43 and 53 are objected to because they include the informality of claim 7.

Claim 8, line 10 and 12, “means” should be deleted (see lines 2 and 3 of claim 8).

Claims 12, 21, 31, 44 and 54 are objected to because they include the informalities of claim 8.

Appropriate correction is required.

Allowable Subject Matter

5. Claims 1, 2, 7, 8, 11, 12, 14, 15, 20, 21, 24, 25, 30, 31, 37, 38, 43, 44, 47, 48, 53, 54 and 57-96 would be allowed if amended to overcome the informalities set forth above (1, 2, 7, 8, 11, 12, 14, 15, 20, 21, 24, 25, 30, 31, 37, 38, 43, 44, 47, 48, 53 and 54) and if upon filing a proper Terminal Disclaimer (1, 2, 14, 15, 24, 25, 37, 38, 47, 48 and 57-64).

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Claims 1, 2, 57, 61, 75 and 80 are allowed because applicant's arguments are found persuasive that the prior art of record fails to disclose or suggest the limitation, in combination with other limitations in the claims, the first potential (inputted to a second electrode of the capacitor) is one of a high level and a low level of the digital signal since the closest prior art (Tam, USP 6,628,146) discloses a first potential (ground which is 0V) rather than one of the high level and the low level of the digital input signal (the input as shown in Figures 4 and 5 takes on a low level of approximately 0.5V and a high level of approximately 1.5V).

Claims 14, 24, 37 and 47 would be allowed because they depend on claim 1.

Claims 15, 25, 38 and 48 would be allowed because they depend on claim 2.

Claims 58-60, 62-64, 76-79 and 81-89 would be allowed because they depend on claims 57, 61, 75 and 80, respectively.

Claims 7, 65 and 85 would be allowed because the prior art of record fails to disclose or suggest, in combination with other limitations, a circuit including first and second capacitors, wherein the switch is turned on and a first potential is input to the second electrode of the first capacitor and a second potential is input to the fourth electrode of the second capacitor during a reset period, and wherein the digital signal is input to the second electrode of the first capacitor and to the fourth electrode of the second capacitor during a sampling period after the reset period as recited in the claims.

Claims 11, 20, 30, 43 and 53 would be allowed because they depend on claim 7.

Claims 66-69 and 86-90 would be allowed because they depend on claims 65 and 85, respectively.

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Claims 8, 70 and 91 would be allowed because the prior art of record fails to disclose or suggest, in combination with other limitations, a circuit including first and second capacitors, wherein the first and second switches are turned on to input a first potential to the second electrode of the first capacitor while the fourth switch is turned on to input a second potential to the fourth electrode of the second capacitor during a reset period, and wherein the third switch is turned on to input the digital signal to the second electrode of the first capacitor while the fifth switch is turned on to input the digital signal to the fourth electrode of the second capacitor during a sampling period after the reset period as recited in the claims.

Claims 12, 21, 31, 44 and 54 would be allowed because they depend on claim 8.

Claims 71-74 and 92-96 would be allowed because they depend on claims 70 and 91, respectively.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

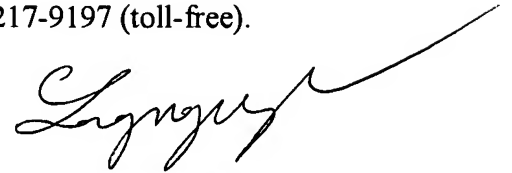
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system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private

PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Long Nguyen', with a long, sweeping horizontal line extending to the right.

LONG NGUYEN
PRIMARY EXAMINER